What is claimed is:

1. A signal amplifier comprising:

an inverter circuit comprised of sub-inverters connected to each other in multiple stages and made up of p-channel transistors and n-channel transistors;

a reference circuit having a circuit configuration corresponding to said inverter circuit and comprised of sub-inverters connected to each other in multiple stages and made up of p-channel transistors and n-channel transistors;

a selection circuit for independently selecting the p-channel transistor and the n-channel transistor from each other with the same combination as the combination of the selection of the p-channel and n-channel transistors in said inverter circuit and reference circuit; and

a selection control circuit for comparing a first driving capacity serving as a driving capacity of the p-channel transistor selected in said reference circuit with a second driving capacity serving as a driving capacity of the n-channel transistor selected in said reference circuit, and outputting a control signal to said selection circuit so as to achieve a balance between the first driving capacity and the second driving capacity based on the result of comparison, thereby controlling said selection signal;

wherein said selection circuit controls operations of the p-channel transistors and the n-channel transistors in said

inverter circuit in response to an input signal of said inverter circuit and the control signal outputted from the selection control circuit.

2. A signal amplifier according to Claim 1, wherein said selection control circuit comprises:

a comparator circuit for comparing the first driving capacity serving as the driving capacity of the p-channel transistor selected in said reference circuit with the second driving capacity serving as the driving capacity of the n-channel transistor selected in said reference circuit;

a decision circuit for deciding as to whether either the number of selection of the p-channel transistors or the number of selection of the n-channel transistors is changed on the basis of the result of comparison in the comparator circuit; and

a selection increment/decrement circuit for controlling said selection circuit so as to change either the number of selection of the p-channel transistors or the number of selection of the n-channel transistors on the basis of the result of decision in the decision circuit.

3. A signal amplifier according to Claim 2, wherein said decision circuit comprises first and second counter circuits either of count values of which is incremented in response to the result of comparison;

said selection increment/decrement circuit comprises a

first selection decode circuit for changing the number of selection of the p-channel transistors in response to the count value of the first counter circuit and a second selection decode circuit for changing the number of selection of the n-channel transistors in response to the count value of the second counter circuit.

4. A signal amplifier according to Claim 3, wherein said first counter circuit increments a count value when the first driving capacity is high on the basis of the result of comparison, and said first selection decode circuit controls said selection circuit so as to decrease the number of selection of the p-channel transistors in response to the count value of the first counter circuit; and

wherein said second counter circuit increments a count value when the second driving capacity is high on the basis of the result of comparison, and said second selection decode circuit controls said selection circuit so as to decrease the number of selection of the n-channel transistors in response to the count value of the second counter circuit.

5. A signal amplifier according to Claim 3, wherein said second counter circuit increments a count value when the first driving capacity is high on the basis of the result of comparison, and said second selection decode circuit controls said selection circuit so as to increase the number of selection of the n-channel transistors according to the count value of the

second counter circuit;

and wherein said first counter circuit increments a count value when the second driving capacity is high on the basis of the result of comparison, and said first selection decode circuit controls said selection circuit so as to increase the number of selection of the p-channel transistors according to the count value of the first counter circuit.

6. A signal amplifier according to Claim 1, wherein said signal amplifier is a D-class signal amplifier.

7. A signal amplifier according to Claim 1, wherein said inverter circuit is comprised of CMOS inverters connected to each other in multiple stages.